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DESIGN AND ANALYSIS OF LOW POWER BACK-GATED CNTFET SRAM MEMORY CELL OPERATING IN SUB THRESHOLD REGION

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ABSTRACT

While designing supporting and peripheral circuits like address decoders, sensing circuits, sensing amplifiers, pre charge and I/O control circuits are very important for the proper functioning of SRAM. BL and BL are the two access lines present in the SRAM memory cell which is accessed by the supporting circuits. Designing memory cell with low power consumption and high noise margin without compromising propagation delay is a very challenging engineering. In order to maintain performance, however, this has required a corresponding reduction in the transistor threshold voltage. The previous papers deal with memory cell designing using the CNTFET threshold region. By introducing body bias for the transistors, the power and the other characteristics of the memory is changed. This work explains with low supply voltage compared other works of CNTFET SRAM operating in sub threshold region.

Keywords: Carbon Nanotube Field Effect Transistor, SRAM design, Back gate, sub threshold region, low power

1. INTRODUCTION

VLSI and CMOS technology has been scale down to improve the performance. When technology scaled down, standby power consumption increases exponentially with the decrease of threshold voltage of MOSFET devices. While designing SRAM care to be taken at the power dissipation.

CNTFET among other new materials is promising due to the unique one-dimensional band-structure which reduces backscattering and makes near-ballistic operation exceptional electrical properties such as high speed, high-K compatibility, chemical stability, have provided CNTFETs with excellent characteristics which can be used as a channel in Si-based MOSFETs. Similar to the silicon device the CNTFET has four terminals, a dielectric film is wrapped around a portion of the undopped semiconducting nano tube, and a metal gate surrounds the dielectric. The parameters such as pitch, channel length (Lch), gate width (Wgate), and number of tubes will affect the performance of CNTFET. CNT diameter determines the threshold voltage of the CNTFET.

The impact of back gate biasing on SRAM cell is discussed on this paper. This work describes the new design of CNTFET-based SRAM operated in the sub threshold region using optimum back gate biasing scheme for each transistor. We discuss about the operation of SRAM in very low supply voltage compared with conventional SRAM, for this purpose we operate SRAM in sub threshold region.

2. CARBON NANOTUBE FET

Because of high thermal and electrical conductivity CNT are widely used in field effect transistors. The intrinsic mechanical and transport properties of Carbon Nanotubes make them the ultimate carbon fibers. Overall, Carbon Nanotubes show a unique combination of stiffness, strength, and tenacity compared to other fiber materials which usually lack one or more of these properties.

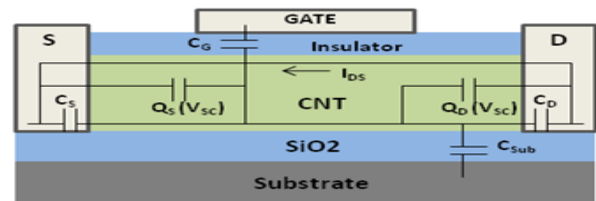

Fig: 1 parasitic effect of CNTFET

Single walled carbon nanotubes (SWCNTs) highly used in applications of electronics because of both their metallic and semiconducting properties and their ability to carry high current. CNTs can carry current density of the order 10 µA/nm2, while standard metal wires have a current carrying capability of the order 10 nA/nm2. Semiconducting CNTs have been used to fabricate CNTFETs, which show promise due to their superior electrical characteristics over silicon based MOSFETs. Since the electron mean free path in SWCNTs can exceed 1 micrometer, long channel CNTFETs exhibit near-ballistic transport characteristics, resulting in high-speed devices. The first CNTFET was fabricated in 1998.
The broad classifications of CNTFET are discussed below.

1. Back-gate CNTFET

In this structure a single SWCNT was used to bridge two noble metal electrodes prefabricated by lithography on an oxidized silicon wafer. Here the SWCNT plays the role of channel and the metal electrodes act as source and drain. The heavily doped silicon wafer itself behaves as the back gate. (of ratio~105). This suffers from some of the limitations like high parasitic contact resistance (≥1Mohm), low drive currents (a few Nano amperes), and low trans conductance gm ≈ 1nS [3]. To reduce these limitations the next generation CNTFET developed which is known as top gate CNTFET.

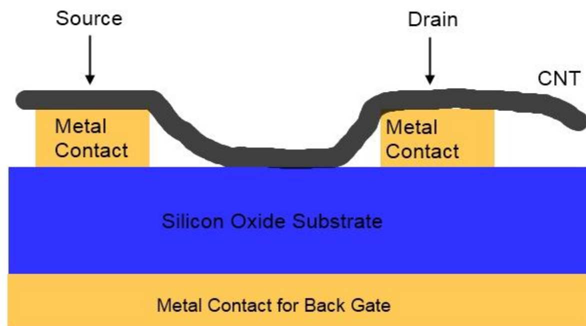

Fig: 2 Top Gated CNTFET

2. Top gate CNTFET

The figure 2 shows the Top gated CNTFET. To get better performance Wind et al. proposed the first top gate CNTFET in 2003[4s. A 15-nm SiO2 film was used as the gate oxide. Here gate is placed over the CNT. The advantage of top gated CNTFET over back gated CNTFET

Advantages and disadvantages of CNTFET

Carbon nanotubes provide better Control over channel formation in FET design, provide better threshold voltage, also better sub threshold conduction, and apart from these CNTFET are higher in speed and current density.

Disadvantages

The carbon nanotube degrades in a few days when exposed to oxygen. There has been several works done on passivating the nanotubes with different polymers and increasing their lifetime.

Difficulties in mass production, production cost

Although CNTs have unique properties such as stiffness, strength, and tenacity compared to other materials especially to silicon, there is a practical problem that, lack of technology for mass production and high production cost. To overcome the fabrication difficulties, several research works have been studied such as direct growth, solution dropping, and various transfer printing techniques.

3. CNTFET SRAM

A typical SRAM cell shown in figure 3 is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (MN3, MN4, MP5, and MP6) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations. A metallic carbon nanotube (CNT) is a tolerant CNTFET memory.

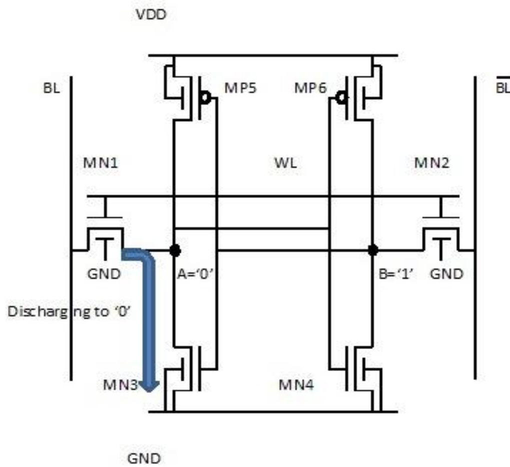

Fig: 3 Conventional SRAM of reading '0'

Access to the cell is enabled by the word line (WL in figure 3) which controls the two access transistors MN1 and MN2 which, in turn, control whether the cell should be connected to the bit lines: BL and BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs—in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bit line to swing upwards or downwards.

If the word line is not asserted, the access transistors MN1 and MN2 disconnect the cell from the bit lines. The two cross-coupled inverters formed by MN3 – MN6 will continue to reinforce each other as long as they are connected to the supply. Assume that the content of the memory is a **1**; the read cycle is started by precharging both the bit lines to a logical **1**, then asserting the word line WL, enabling both the access transistors.

The second step occurs when the value stored is transferred to the bit line by leaving BL at its precharged value and discharging **BL** through MN1and MN3 to a logical. On the BL side, the transistors MP6 and MN2 pull the bit line toward V_{DD}, a logical **1.**

Figure 3 shows the content of the memory was a **0**, the opposite would happen and **BL** would be pulled toward **1** and BL toward **0**. Then these BL and **BL** will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was **1** stored or **0**. The higher the sensitivity of sense amplifier, the faster the speed of read operation is.

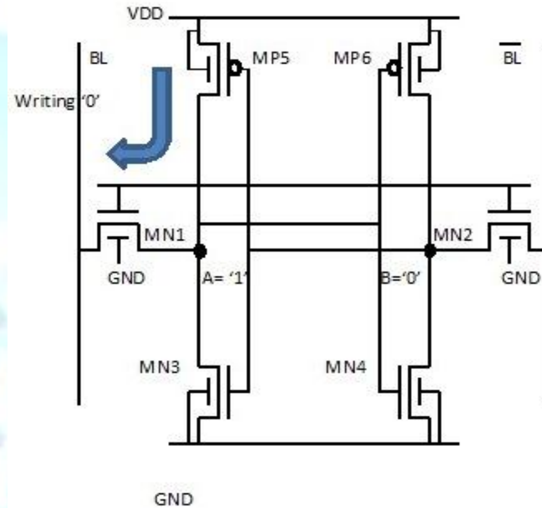

Fig: 4 Writing '0' operation of SRAM

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a **0**, (from figure 4) we would apply a **0** to the bit lines, i.e. setting **BL** to **1** and BL to **0**. This is similar to applying a reset pulse to a SR latch, which causes the flip flop to change state. A **1** is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

Effect of Back gate biasing in CNTFET

The body effect describes the changes in the threshold voltage by the change in V_{SB}, the source-bulk voltage. Since the body influences the threshold voltage (when it is not tied to the source), it can be thought of as a second gate, and is sometimes referred to as the "back

gate"; the body effect is sometimes called the "back-gate effect". For an enhancement mode, n-mos MOSFET body effect upon threshold voltage is computed according to the Shichman-Hodges model (accurate for very old technology) using the following equation.

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|}\right) \quad \text{-- (1)}$$

where V_{TN} is the threshold voltage when substrate bias is present, V_{SB} is the source-to-body substrate bias, 2ØF is the surface potential, and V_{TO} is threshold voltage for zero substrate bias,

$$\gamma = (t_{ox}/\epsilon_{ox})\sqrt{2q\epsilon_{si}N_A} \quad \text{-- (2)}$$

is the body effect parameter, t_{ox} is oxide thickness, ϵ_{ox} is oxide permittivity, ϵ_{si} is the permittivity of silicon, N_A is a doping concentration, q is the charge of an electron.

$$\phi_f = (kT/q)\ln(N_A/N_i) \quad \text{--- (3)}$$

Where k is Boltzmann's constant, T is Temperature, q is the charge of an electron, N_A is a doping parameter and N_i is the intrinsic doping parameter for the substrate.

The threshold voltage of a MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. The formation of the inversion layer allows the flow of electrons through the gate-source junction. The creation of this layer is described next. To prove the effectiveness of back gate biasing, we simulate the Id-Vg characteristic for different back gate biasing voltages for NCNTFET using HSPICE. We use 16nm technology for CNTFET device.

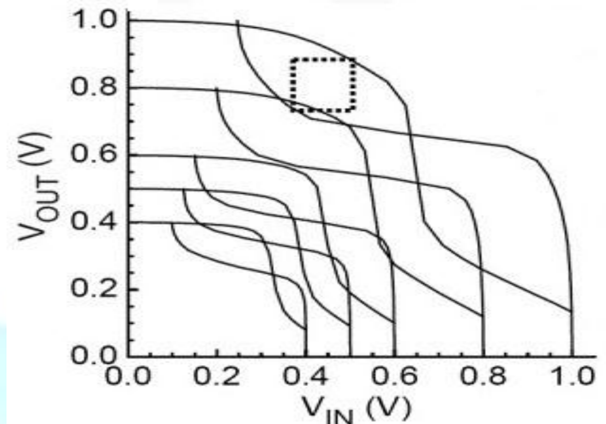

Figure: 5 Logic threshold voltages at different back gate biasing

Fig. 5 shows the logic threshold voltages at different bias voltages of MP5: 0.3V, 0.4 V and 0.5V. Ideal logic threshold voltage for stability is Vdd/2. Therefore, back gate biasing voltage for MP5 is 0.3V considering the stability of the SRAM cell as it is shown in Fig. 6.

From the Fig.6 the proposed CNTFET SRAM cell structure. In the proposed CNTFET SRAM cell structure, each transistor can be back gate biased dynamically according to the operation modes. Assuming A stores "1" in read mode and B is "0".

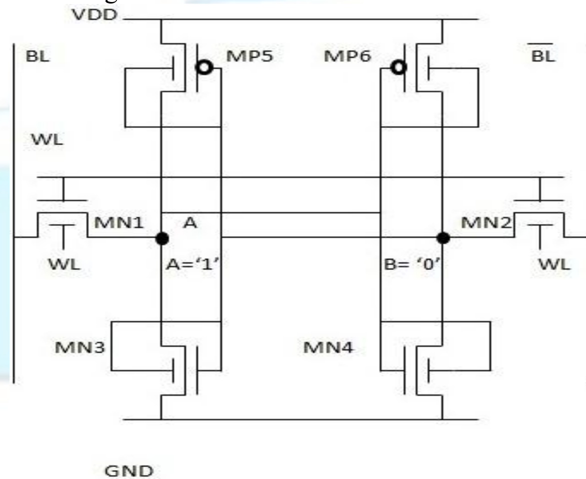

Fig: 6 Proposed CNTFET SRAM with back-gate

	Read1	Read0	Write1	Write0
MN 1	Vbb=Vdd	Vbb=Vdd	Vbb=Vdd	Vbb=Vdd
MN 2	Vbb=Vdd	Vbb=Vdd	Vbb=Vdd	Vbb=Vdd
MN 3	Vbb=0V	Vbb=Vdd	Vbb=0V	Vbb=0V
MN 4	Vbb=Vdd	Vbb=0V	Vbb=0V	Vbb=0V
MP 5	Vbb=0V	Vbb=Vdd	Vbb=Vdd	Vbb=Vdd
MP 6	Vbb=Vdd	Vbb=0V	Vbb=Vdd	Vbb=Vdd

Table 1 summaries the proposed back gate biasing schemes for CNTFET SRAM cell, the transistors operating in sub threshold region.

transistor MN3 and MP5 will be zero biased because of the connection between the A node and the back gate terminals of MN3 and MP5. If A stores "0" in read mode, MN3 and MP5 will be forward biased. The same operation can be made for MN4 and MP6 during read mode. Therefore, according to table 1, the SRAM cell shown in Fig. 6 has optimum back gate biasing scheme at read mode. During write mode, depending on the voltages of A and B, MN3, MP5, MN4 and MP6 will be forward biased or zero biased, which is the sub-threshold biasing scheme for write mode. In hold mode, the transistors which are off are zero biased. For example, in hold mode, A stores 1 and B is 0, MN3 is off and MP5 is on. The back gate biasing voltage for MN3 is 0. Even though MP5 is forward biased, MN3 is the main source for static power consumption. Therefore, the proposed CNTFET SRAM cell structure provides the better back gate biasing scheme in hold mode as well as in read mode.

	Noise Margin(V)	Power
Traditional CNTFET SRAM	0.03	0.157nw
Back-gated CNTFET SRAM	0.106 (increased)	0.132nw (decreased)

Table 2 shows that the proposed sub threshold SRAM cell reduces power 52% and increases WNM 2.3X compared with traditional sub threshold CNTFET

5. CONCLUSION

This work uses very low supply voltage compared with conventional SRAM so that the total power consumption used by the memory is reduced. We use 0.7V as the VDD for the back gated bias and 1V for normal mode operation and analyzed the two results. By using this concept we can design the memory cell with very low power consumption, reduced propagation delay, increased noise margin. The proposed back-gate biased CNTFET SRAM cell consumes less power compared to traditional CNTFET SRAM. The table 2 shows the comparison of power and noise margin with and without back-gate biasing of SRAM. From the comparison, the propose CNTFET SRAM reduce the power of 52% and increase the voltage noise margin of nearly two times. We simulated the SRAM circuit using HSPICE software with 4 nanotubes for a FET. The same performance can be obtained by reducing number of nano tubes to half.

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